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Method of fabricating flash memory device

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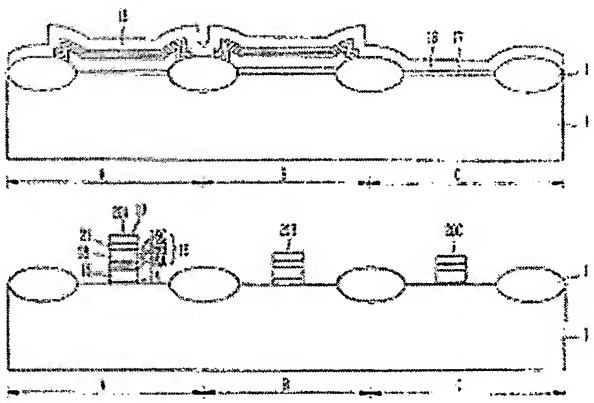
The present invention discloses a method of fabricating a flash memory device. In the present invention, since the dielectric film formed in the memory cell region is only exposed to the cleaning solution which is used in cleaning process preformed after removing the dielectric film formed in the low voltage transistor region, the number of damages applied to the dielectric film can be minimized, therefore, a good dielectric film can be obtained.



Description of corresponding document: **US5888869**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of fabricating a flash memory device, and more particularly to method of fabricating a flash memory device which can minimize damage of a dielectric film in the process of forming a high voltage transistor and a low voltage transistor having gate electrode consisted

a polysilicon layer and a silicide layer.

2. Brief Description of the Prior Art

Generally, in a memory device, a gate electrode must have a two-layer structure of a polysilicon layer a a silicide layer for realizing a high programming and an erasure operations, and also a low voltage transistor having a gate oxide film with a thickness of 30 to 150 .ANG. and a high voltage transistor hav a gate oxide film with a thickness of 150 to 300 .ANG. are formed in the flash EEPROM cell.

Then, a method of fabricating a conventional flash memory device comprising a high voltage and low voltage transistors which have gate electrode consisted of a polysilicon layer/a silicide layer, respectivel will be explained below in detail by reference to the accompanying drawings.

FIGS. 1A through 1L are sectional views for illustrating step by step a method of fabricating a conventional flash memory device.

An oxide film 3 is formed on a silicon substrate 1 which is divided into a memory cell region A, a high voltage transistor region B and a low voltage transistor region C by field oxide films 2 (FIG. 1A).

The oxide film 3 in a memory cell region A is removed so that the silicon substrate 1 in the memory cel region A is exposed (FIG. 1B). A tunnel oxide film 4 is formed in the memory cell region A, a first polysilicon layer 5 is then formed on the entire structure including the field oxide films 2 (FIG. 1C). Th the first polysilicon layer 5 formed on the high voltage and the low voltage transistors regions B and C i removed, therefore, the first polysilicon layer 5 on the tunnel oxide film 4 is remained (FIG. 1D).

A dielectric film 6 having ONO structure of a lower oxide film 6A, a nitride film 6B and a upper oxide film 6C is formed on the entire structure including the field oxide layers 2 (FIG. 1E). And then, the dielectric film 6 formed in the high voltage and the low voltage transistor regions B and C is selectively removed, and the first cleaning process is performed (FIG. 1F). Then, ions are injected in the high volta and the low voltage transistors B and C and the second cleaning process is performed. The oxide film 3 formed in the high voltage and the low voltage transistors B and C is removed by use of HF (FIG. 1G). this time, as can be seen from FIG. 1G, the upper oxide film 6C of the dielectric layer 6 formed in the memory cell region A is also removed in the process of removing the oxide film 3 by use of HF.

An then, a middle oxide film 6D is formed on the entire structure except for the field oxide films 2 (FIG 1H), the middle oxide film 6D formed in the memory cell region A and the ow voltage transistor region is removed and the third cleaning process is performed (FIG. 1I). During the third cleaning process, the nitride film 6B of the dielectric film 6 formed in the memory cell region A is damaged.

Then, a gate oxide film 7 is formed in the low voltage transistor region C. At this time, an upper oxide f 6C is formed again on the nitride film 6B, therefore, the dielectric film 6 having an ONO structure is formed in the memory cell region A.

A second polysilicon layer 8 and a silicide layer 9 are sequentially formed on the entire structure includi the field oxide film 2 (FIG. 1K), the second polysilicon layer 8 and the silicide layer 9 are patterned so g electrodes 10B and 10C are formed in the high voltage and the low voltage transistors B and C (FIG. 1L A gate electrode 10A is formed in the active region of the memory cell region A by patterning process.

As described above, in the process of forming the gate electrodes 10A, 10B and 10C in the memory cell region A, the high voltage transistor region B and the low voltage transistor region C, respectively, the dielectric film 6 formed in the memory cell region A is damaged by cleaning solutions which is used fo

the cleaning processes. Therefore, the characteristic of the device is degraded.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a method of fabricating a flash memory device which can form an uniform dielectric film without damage in the process of forming a gate electrode.

In order to achieve to above object, the present invention comprises steps of forming an oxide film on a silicon substrate divided into a memory cell region, a high voltage transistor region and a low voltage transistor region by field oxide films; removing the oxide film formed in the memory cell region and forming a tunnel oxide film on the exposed silicon substrate; forming a first polysilicon layer on the ent structure including the field oxide films and removing some of the first polysilicon layer to remain the f polysilicon layer in active regions of the memory cell region and the high voltage transistor region; forming a dielectric film having an ONO structure on the entire structure including the field oxide films removing the dielectric film formed in the low voltage transistor region and performing a cleaning proc forming a gate oxide film in the low voltage transistor region and forming a second polysilicon layer on the entire structure; removing the second polysilicon layer and the dielectric film formed in the high voltage transistor region and performing a cleaning process; sequentially forming a third polysilicon lay and a silicide layer on the entire structure; forming gate electrodes in the memory cell region, the high voltage transistor region and the low voltage transistor region by patterning process, respectively. The t polysilicon layer may not be formed if a thickness of the first and second polysilicon layers and is enou

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the present invention will be understood by reading the detailed explanation of the embodiment with reference to the accompanying drawings in which:

FIGS. 1A through 1M are sectional views of device for illustrating a conventional method of fabricating flash memory device.

FIGS. 2A through 2K are sectional views of device for illustrating a method of fabricating a flash memc device in accordance with the present invention.

DESCRIPTION OF THE INVENTION

The present invention will be described below in detail by reference to the accompanying drawings.

FIGS. 2A through 2K are sectional views of device for illustrating a method of fabricating a flash memc device in accordance with the present invention.

An oxide film 13 is formed on a silicon substrate 11 which is divided into a memory cell region A, a hig voltage transistor region B and a low voltage transistor region C by field oxide films 12 (FIG. 2A). The oxide film 13 formed in the memory cell region A is removed so that the silicon substrate 11 is exposed and a tunnel oxide film 14 is formed on the exposed silicon substrate 11 (FIG. 2B). Then a first polysili layer 15 is formed on the entire structure including the field oxide films 12 (FIG. 2C), and some of the f polysilicon layer 15 is removed to remain the first polysilicon layer 15 in the active regions of the memc cell region A and the high voltage transistor region B (FIG. 2D).

A dielectric film 16 having ONO structure of a lower oxide film 16A, a nitride film 16B and an upper oxide film 16C is formed on the entire structure including the field oxide films 12 (FIG. 2E). Thereinaft

the dielectric film 16 formed in the low voltage transistor region C is removed, and then a cleaning proc is performed (FIG. 2F). At this time, the upper oxide film 16C of the dielectric film 16 formed in the memory cell region A is damaged by a cleaning solution.

A gate oxide film 17 is formed in the low voltage transistor region C, and a second polysilicon layer 18 formed on the entire structure (FIG. 2G). Then, the second polysilicon layer 18 and the dielectric film 1(which are formed in the high voltage transistor region B are sequentially removed, and then a cleaning process is performed (FIG. 2H).

A third polysilicon layer 21 and a silicide layer 19 is formed sequentially on the entire structure (FIG. 2I A gate electrode 20B consisted of the oxide film 13, the first polysilicon layer 15 the third polysilicon la 21 and the silicide layer 19 is formed in the high voltage transistor region B, and a gate electrode 20C consisted of the gate oxide film 17, the second polysilicon layer 18, the third polysilicon layer 21 and th silicide layer 19 is formed in the low voltage transistor region C, respectively, by the patterning process. Also, a gate electrode 20A which is consisted of the tunnel oxide film 14, the first polysilicon layer 15, 1 dielectric film 16, the second and third polysilicon layers 18 and 21 and the silicide layer 19 in stacked i formed in the memory cell region A (FIG. 2K) through the patterning process.

As mentioned above, during process for forming gate electrodes 20A, 20B and 20C according to the present invention, since the dielectric film 16 formed in the memory cell region A, especially the upper oxide film 16C, is only exposed to the cleaning solution which is used in cleaning process preformed afi removing the dielectric film formed in the low voltage transistor region C, the number of damages appli to the dielectric film 16 can be minimized, therefore, a good dielectric film can be obtained.

In the above description, although the third polysilicon layer 21 is formed on the second polysilicon lay(18 (at the gate electrodes 20A and 20C) or the first polysilicon layer 15 (at the gate electrode 20B), the third polysilicon layer 21 may not be formed if a thickness of the first and second polysilicon layers 15 ; 18 is enough.

The foregoing description, although described in its preferred embodiments with a certain degree of particularity, is only illustrative of the principle of the present invention. It is to be understood that the present invention is not to be limited to the preferred embodiments disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope and spirit of the present inventi are to be encompassed as further embodiments of the present invention.

Claims of corresponding document: **US5888869**

What is claimed is:

1. A method of fabricating a flash memory device, comprising the sequential steps of:
forming an oxide film on a silicon substrate divided into a memory cell region, a high voltage transistor region and a low voltage transistor region by field oxide films;
removing the oxide film formed in the memory cell region and forming a tunnel oxide film on the expos silicon substrate;
forming a first polysilicon layer on the entire structure including the field oxide films and removing son of the first polysilicon layer to leave the first polysilicon layer in active regions of the memory cell regic and the high voltage transistor region;

forming a dielectric film having an ONO structure on the entire structure including the field oxide films
removing the dielectric film formed in the low voltage transistor region and performing a cleaning proce

forming a gate oxide film in the low voltage transistor region and forming a second polysilicon layer on the entire structure;
removing the second polysilicon layer and the dielectric film formed in the high voltage transistor regio and performing a cleaning process;
sequentially forming a third polysilicon layer and a silicide layer on the entire structure;
forming gate electrodes in the memory cell region, the high voltage transistor region and the low voltag transistor region by patterning process, respectively.

2. A method of fabricating a flash memory device, comprising the sequential steps of:
forming an oxide film on a silicon substrate divided into a memory cell region, a high voltage transistor region and a low voltage transistor region by field oxide films;
removing the oxide film formed in the memory cell region and forming a tunnel oxide film on the expos silicon substrate;
forming a first polysilicon layer on the entire structure including the field oxide films and removing som of the first polysilicon layer to leave the first polysilicon layer in active regions of the memory cell regic and the high voltage transistor region;
forming a dielectric film having an ONO structure on the entire structure including the field oxide films
removing the dielectric film formed in the low voltage transistor region and performing a cleaning proce

forming a gate oxide film in the low voltage transistor region and forming a second polysilicon layer on the entire structure;
removing the second polysilicon layer and the dielectric film formed in the high voltage transistor regio and performing a cleaning process;
forming a third polysilicon layer on the entire structure;
forming gate electrodes in the memory cell region, the high voltage transistor region and the low voltag transistor region by patterning process, respectively.

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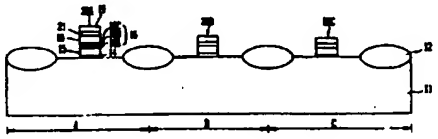
权利要求书 2 页 说明书 4 页 附图页数 12 页

[54]发明名称 闪速存储器件的制造方法

[57]摘要

本发明公开了一种制造闪速存储器件的方法。在本发明中，由于在存储单元区内形成的介质膜仅暴露给清洗溶剂，而该清洗溶剂是用于在除去低压晶体管区内形成介质膜后所实施的清洗工艺中，介质膜受到损伤的数量可减小到最小，因此，可以得到良好的介质膜。



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1. 一种制造闪速存储器件的方法，其特征在于，包括以下步骤:

在由场氧化膜分为存储单元区、高压晶体管区和低压晶体管区的硅衬底上形成氧化膜;

除去在存储单元区内形成的氧化膜并在露出的硅衬底上形成隧道氧化膜;

在包括场氧化膜的整个结构上形成第一多晶硅层并除去部分第一多晶硅层从而在存储单元区和高压晶体管区的有源区内留有第一多晶硅层;

在包括场氧化膜的整个结构上形成有 ONO 结构的介质膜;

除去低压晶体管区内所形成的介质膜并进行清洗工艺;

在低压晶体管区内形成栅氧化膜并在整个结构上形成第二多晶硅层;

除去高压晶体管区内所形成的第二多晶硅层和介质膜并进行清洗工艺;

依次在整个结构上形成第三多晶硅层和硅化物层;

通过图形形成工艺分别在存储单元区、高压晶体管区和低压晶体管区内形成栅电极.

2. 一种制造闪速存储器件的方法，包括以下步骤:

在由场氧化膜分为存储单元区、高压晶体管区和低压晶体管 区的硅衬底上形成氧化膜;

除去在存储单元区内形成的氧化膜并在露出的硅衬底上形成隧道氧化膜;

在包括场氧化膜的整个结构上形成第一多晶硅层并除去部分第一多晶硅层从而在存储单元区和高压晶体管区的有源区内留有第一多晶硅层;

在包括场氧化膜的整个结构上形成有 ONO 结构的介质膜;

除去低压晶体管区内所形成的介质膜并进行清洗工艺;

在低压晶体管区内形成栅氧化膜并在整个结构上形成第二多晶硅层;

除去高压晶体管区内的第二多晶硅层和介质膜并进行清洗工艺;

在整个结构上形成第三多晶硅层;

通过图形形成工艺分别在存储单元区、高压晶体管区和低压晶体管

区内形成栅电极.

说　明　书

闪速存储器件的制造方法

本发明涉及闪速存储器件的制造方法，特别涉及在形成高压晶体管和低压晶体管的工艺中使介质膜损伤最小的闪速存储器件的制造方法，而该高压晶体管和低压晶体管的栅电极包括多晶硅层和硅化物层。

通常，在存储器件中，栅电极必须具有多晶硅层和硅化物层的两层结构，用于实现快速编程和擦除操作，在闪速 EEPROM 单元内还形成栅氧化膜厚度为 30 至 150Å 的低压晶体管和栅氧化膜厚度为 150 至 300Å 的高压晶体管。

下面将结合附图分别对包括高压晶体管和低压晶体管的常规闪速存储器件的制造方法进行详细介绍，而该高压晶体管和低压晶体管的栅电极包括多晶硅层/硅化物层。

图 1A-1L 为按步序介绍常规闪速存储器件的制造方法的剖面图。

在硅衬底 1 上形成氧化膜 3，而该硅衬底由场氧化膜 2 分为存储单元区 A、高压晶体管区 B 和低压晶体管区 C（图 1A）。

去除存储单元区 A 内的氧化膜 3 以便露出存储单元区 A 内的硅衬底 1（图 1B）。在存储单元区 A 内形成隧道氧化膜 4，之后在包括场氧化膜 2 的整个结构上形成第一多晶硅层 5（图 1C）。然后去除在高压和低压晶体管区 B 和 C 上形成的第一多晶硅层 5，因此，隧道氧化膜 4 上的第一多晶硅层 5 被保留下来（图 1D）。

在包括场氧化膜 2 的整个结构上形成具有下氧化膜 6A、氮化膜 6B 和上氧化膜 6C 的 ONO 结构的介质膜 6（图 1E）。之后，有选择性的除去在高压和低压晶体管区 B 和 C 内形成的介质膜 6，并进行第一次清洗工艺（图 1F）。然后，在高压和低压晶体管区 B 和 C 内注入离子，并进行第二次清洗工艺。使用 HF 除去在高压和低压晶体管区 B 和 C 内形成的氧化膜 3（图 1G）。此时，从图 1G 中可看出，在存储单元区 A 内形成的介质膜 6 的上氧化膜 6C 在使用 HF 的去除氧化膜 3 过程中也被

除去。

之后，在除场氧化膜 2 的整个结构上形成中间氧化膜 6D（图 1H），将存储单元区 A 和低压晶体管区 C 内形成的中间氧化膜 6D 除去并进行第三次清洗工艺（图 1I）。在第三次清洗工艺中，在存储单元区 A 内形成的介质膜 6 的氮化膜 6B 受到损伤。

然后，在低压晶体管区 C 内形成栅氧化膜 7。此时，在氮化膜 6B 上再次形成上氧化膜 6C，因此，在存储单元区 A 内形成了具有 ONO 结构的介质膜 6。

依次在除场氧化膜 2 的整个结构上形成第二多晶硅层 8 和硅化物层 9（图 1K），将第二多晶硅层 8 和硅化物层 9 形成图形，所以在高压和低压晶体管区 B 和 C 内形成栅电极 10B 和 10C（图 1L）。通过图形形成工艺在存储单元区 A 的有源区内形成栅电极 10A。

如上所述，在存储单元区 A、高压晶体管区 B 和低压晶体管区 C 内分别形成栅电极 10A、10B 和 10C 的工艺中，在存储单元区 A 内形成的介质膜 6 被用于清洗工艺的清洗溶液损伤。因此，使器件的特性降低。

因此，本发明的目的在于提供一种在形成栅电极工艺中得到没有损伤的均匀介质膜的闪速存储器件的制造方法。

为了达到以上目的，本发明包括以下步骤：在由场氧化膜分为存储单元区、高压晶体管区和低压晶体管区的硅衬底上形成氧化膜；除去在存储单元区内形成的氧化膜并在露出的硅衬底上形成隧道氧化膜；在包括场氧化膜的整个结构上形成第一多晶硅层并除去部分第一多晶硅层从而在存储单元区和高压晶体管区的有源区内留有第一多晶硅层；在包括场氧化膜的整个结构上形成有 ONO 结构的介质膜；除去低压晶体管区内所形成的介质膜并进行清洗工艺；在低压晶体管区内形成栅氧化膜并在整个结构上形成第二多晶硅层；除去高压晶体管区内所形成的第二多晶硅层和介质膜并进行清洗工艺；依次在整个结构上形成第三多晶硅层和硅化物层；通过图形形成工艺分别在存储单元区、高压晶体管区和低压晶体管区内形成栅电极。如果第一和第二多晶硅层的厚度已足够，则不必形成第三多晶硅层。

通过以下结合附图对实施例的详细介绍可更好地理解本发明的其它目的和优点，其中：

图 1A-1L 为制造闪速存储器件的常规方法的剖面图.

图 2A-2K 为依照本发明制造闪速存储器件的方法的剖面图.

下面将结合附图详细介绍本发明.

图 2A-2K 为依照本发明制造闪速存储器件的方法的剖面图.

在硅衬底 11 上形成氧化膜 13，而该硅衬底由场氧化膜 12 分为存储单元区 A、高压晶体管区 B 和低压晶体管区 C（图 2A）. 将存储单元区 A 内所形成的氧化膜 13 除去，以便露出硅衬底 11，在露出的硅衬底 11 上形成隧道氧化膜 14（图 2B）. 在包括场氧化膜 12 的整个结构上形成第一多晶硅层 15（图 2C），除去部分第一多晶硅层 15 从而在存储单元区 A 和高压晶体管区 B 的有源区内留有第一多晶硅层 15（图 2D）.

在包括场氧化膜 12 的整个结构上形成具有下氧化膜 16A、氮化物膜 16B 和上氧化膜 16C 的 ONO 结构的介质膜 16（图 2E）. 此后，除去在低压晶体管区 C 内形成的介质膜 16，之后进行清洗工艺（图 2F）. 此时，在存储单元区 A 内形成的介质膜 16 的上氧化膜 16C 被清洗溶液损伤.

在低压晶体管区 C 内形成栅氧化膜 17，并在整个结构上形成第二多晶硅层 18（图 2G）. 然后依次除去高压晶体管区 B 内的第二多晶硅层 18 和介质膜 16 并进行清洗工艺（图 2H）.

在整个结构上依次形成第三多晶硅层 21 和硅化物层 19（图 2I）. 在高压晶体管区 B 内形成由氧化膜 13、第一多晶硅层 15、第三多晶硅层 21 和硅化物层 19 构成的栅电极 20B，通过图形形成工艺分别在低压晶体管区 C 内形成由栅氧化膜 17、第二多晶硅层 18、第三多晶硅层 21 和硅化物层 19 构成的栅电极 20C. 同样，通过图形形成工艺在存储单元区 A 内形成由隧道氧化膜 14、第一多晶硅层 15、介质膜 16、第二

和第三多晶硅层 18 和 21 及硅化物层 19 堆叠构成的栅电极 20A（图 2K）。

如上所述，在根据本发明形成栅电极 20 A、20B 和 20C 的工艺中，由于在存储单元区 A 内形成的介质膜 16，特别是上氧化层 16C，仅暴露给清洗溶剂，而该清洗溶剂是在除去低压晶体管区 C 内形成介质膜后所实施的清洗工艺中使用的，介质膜 16 受到损伤的数量可减小到最小，因此，可以得到良好的介质膜。

在以上的说明中，虽然第三多晶硅层 21 被形成在第二多晶硅层 18（栅电极 20 A 和 20C 处）或第一多晶硅层 15（栅电极 20B 处）上，如果第一和第二多晶硅层 15 和 18 的厚度已足够，则不必形成第三多晶硅层 21。

前面的说明，虽然在对优选实施例的说明中带有某种程度的特殊性，但这仅是对本发明的原理的说明。应该理解本发明并不局限在这里公开和图示的优选实施例。在本发明的范围和精神内做出的适当变形都将包括在本发明的另外的实施例中。

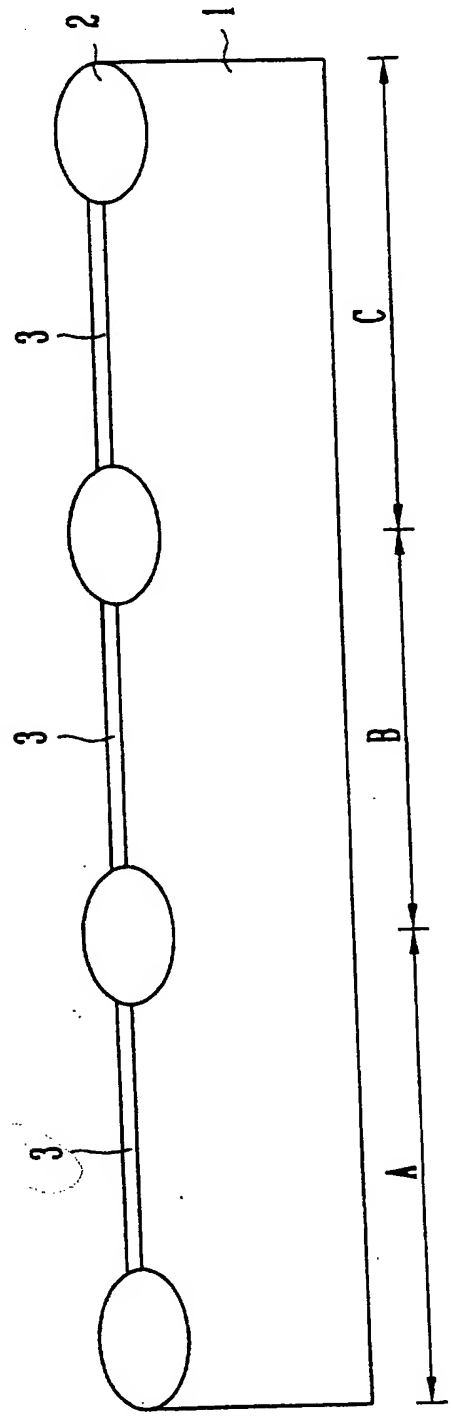


图 1A （现有技术）

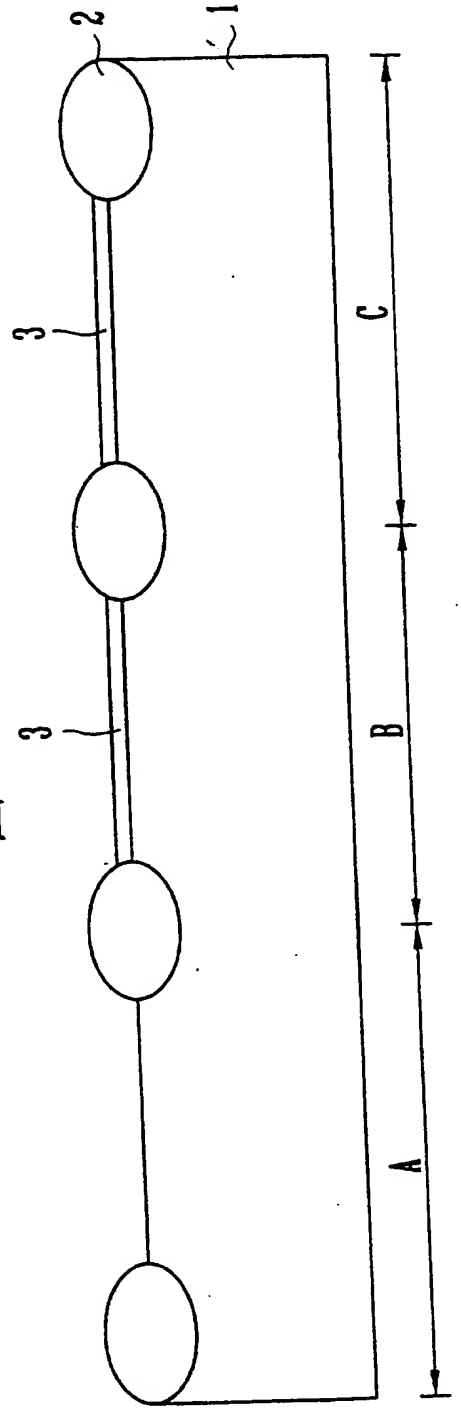


图 1B （现有技术）

图 1C（现有技术）

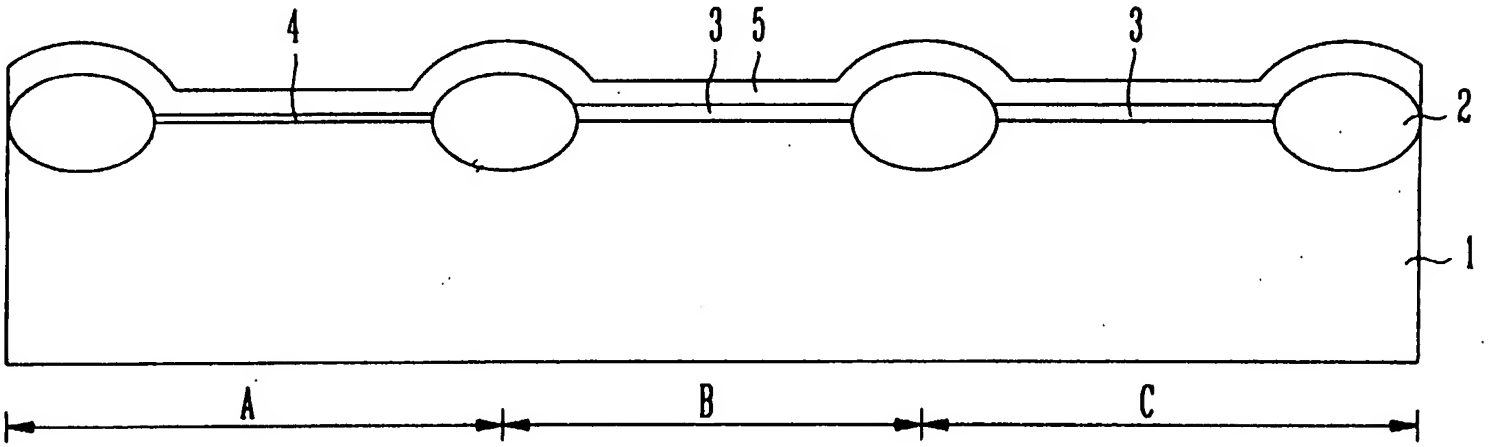


图 1D （现有技术）

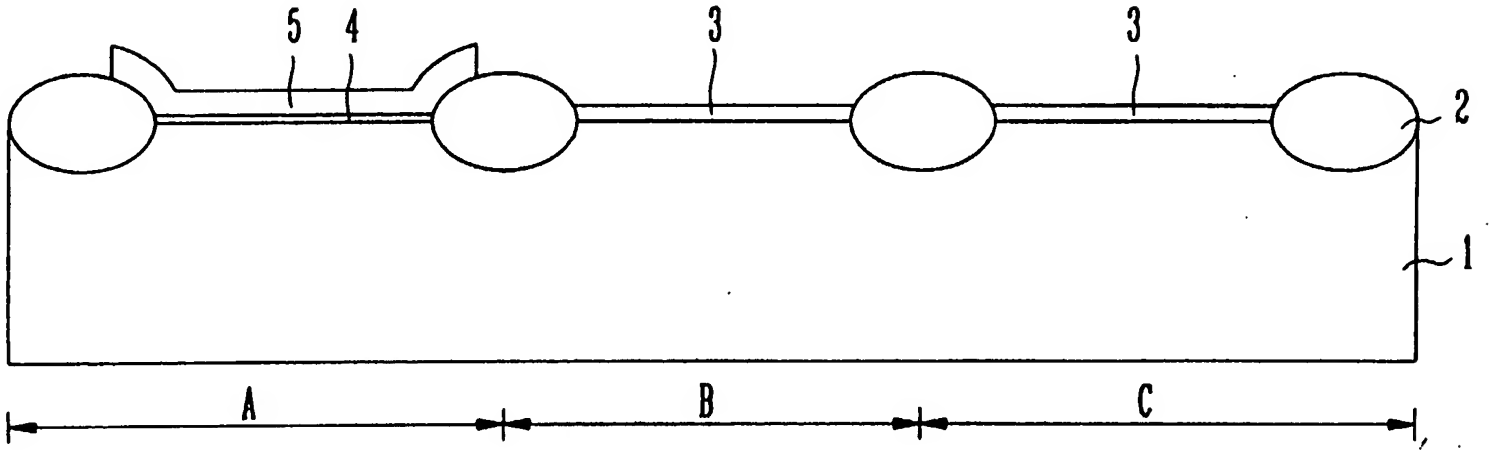


图 1E（现有技术）

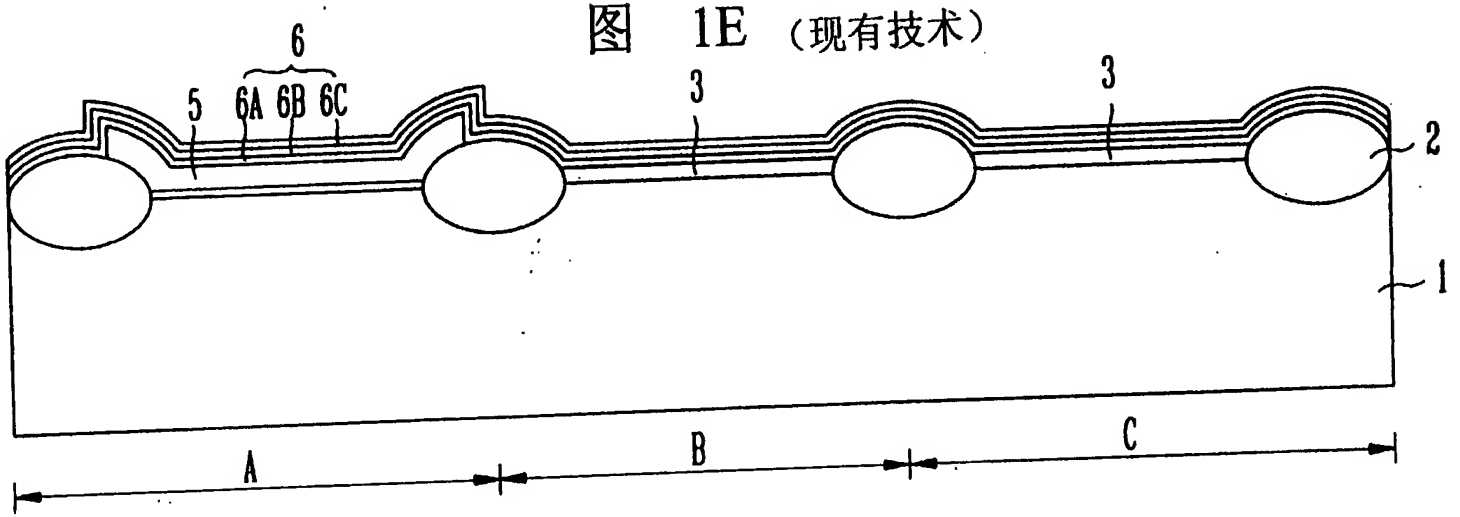


图 1F（现有技术）

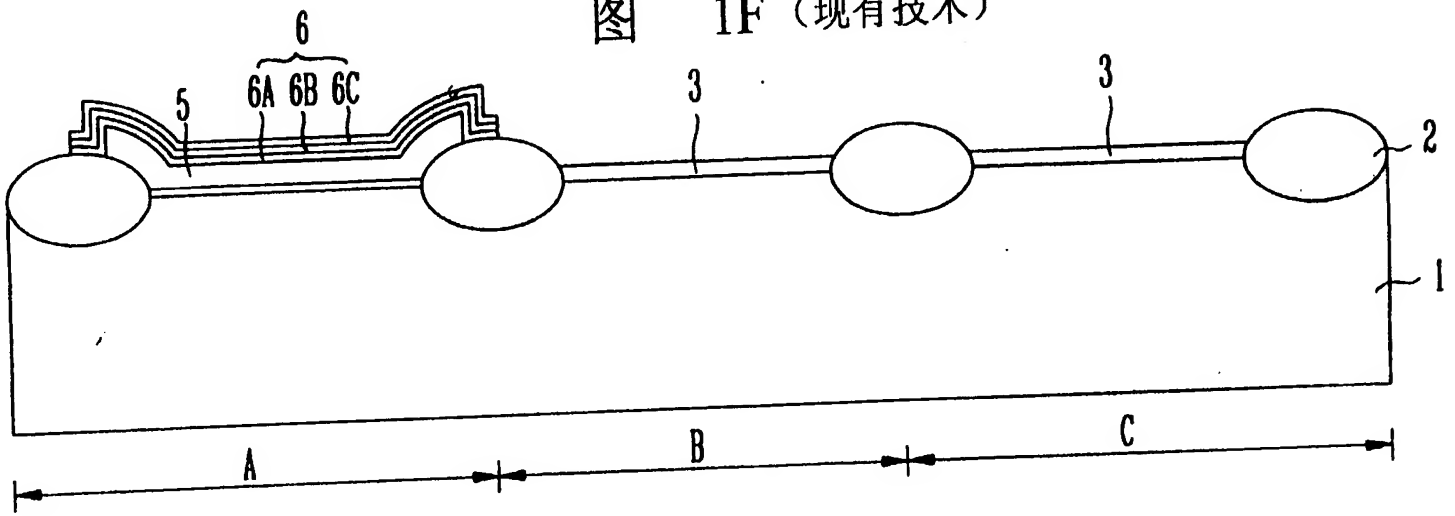


图 1G （现有技术）

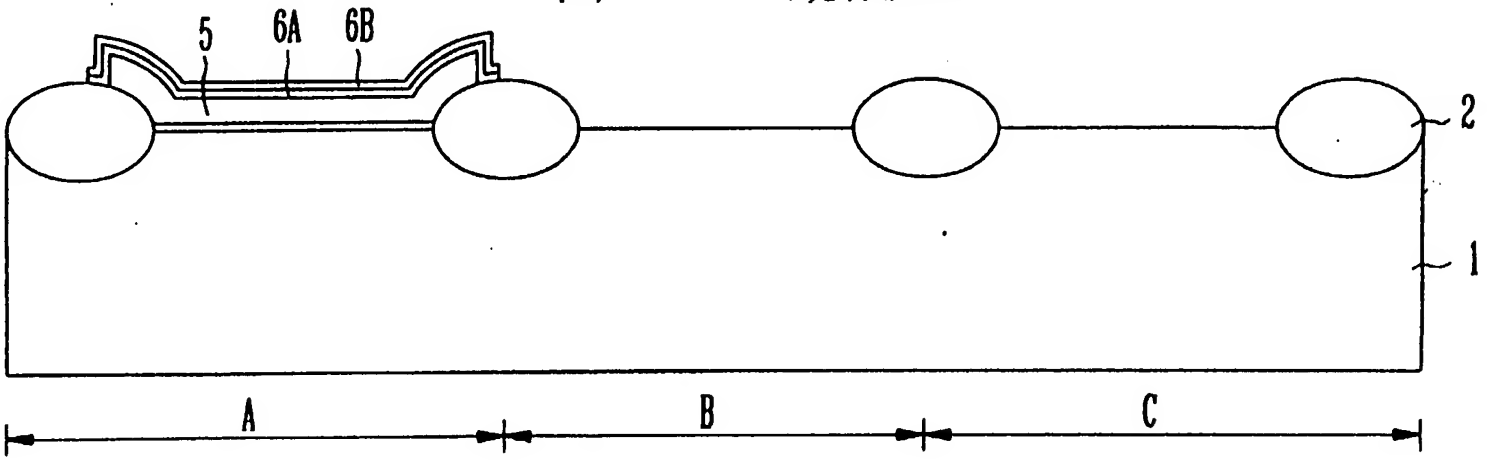


图 1H （现有技术）

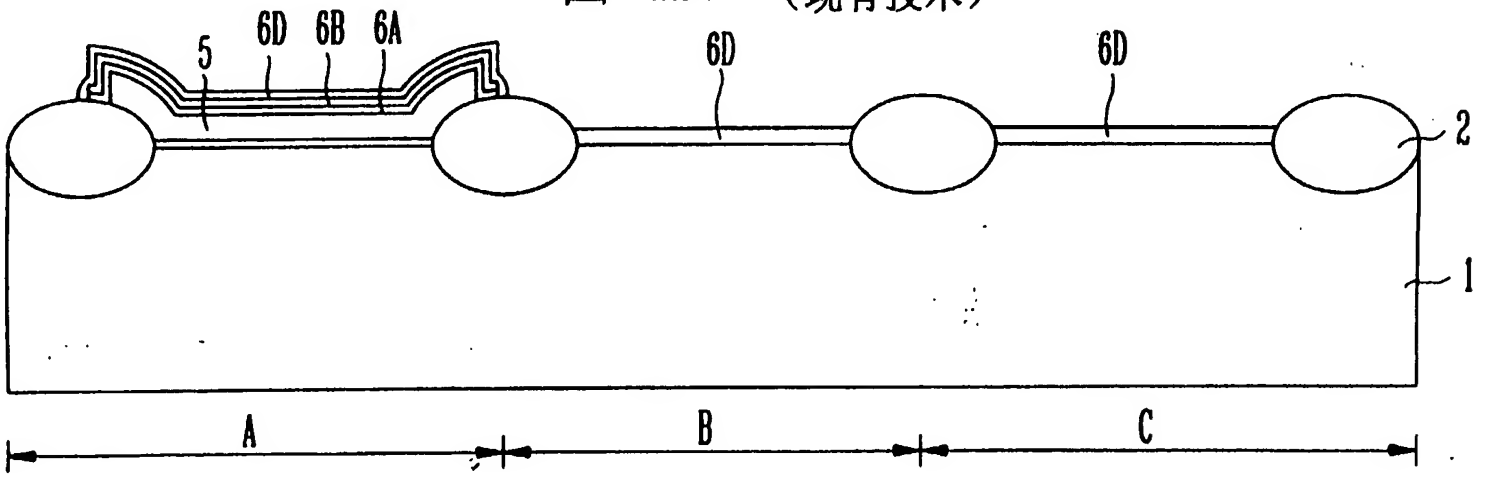


图 1I （现有技术）

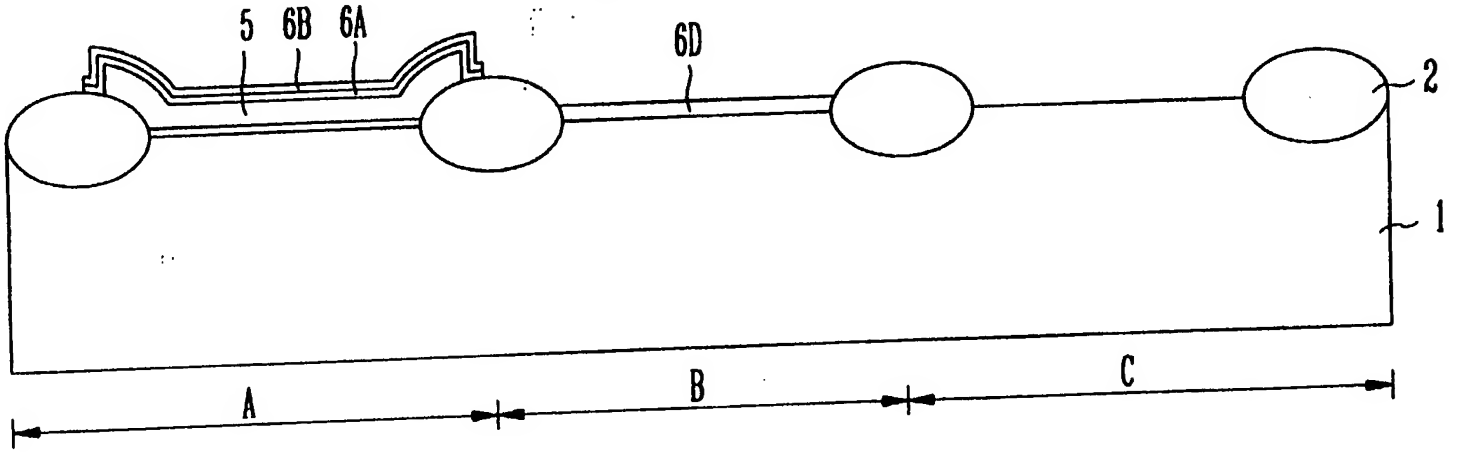


图 1J （现有技术）

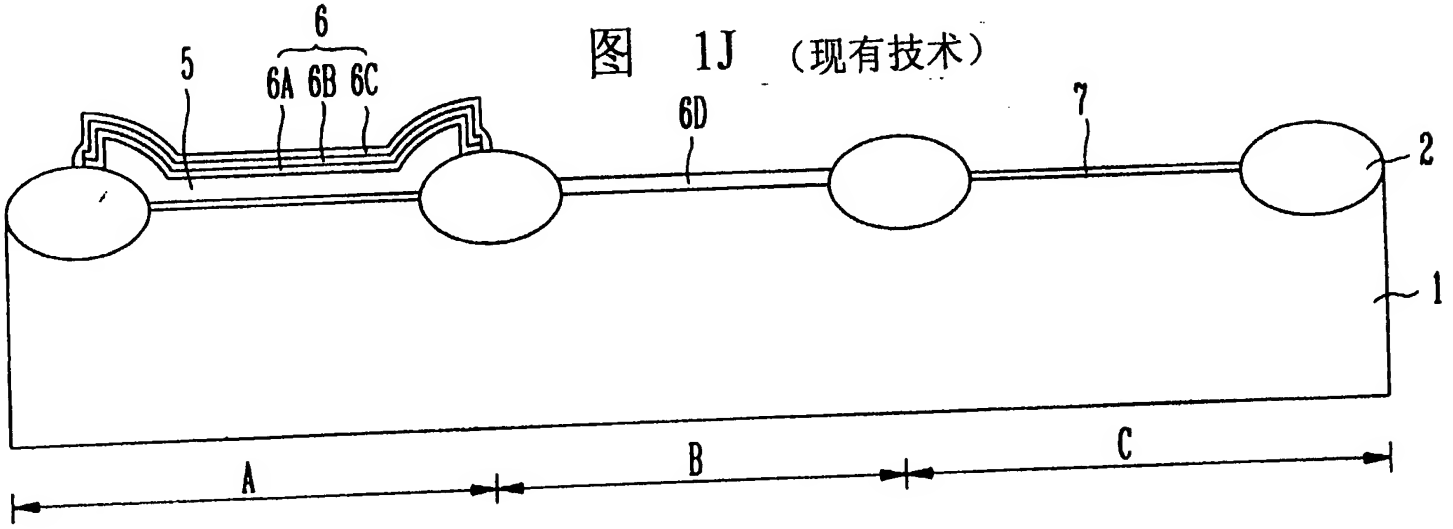


图 1K （现有技术）

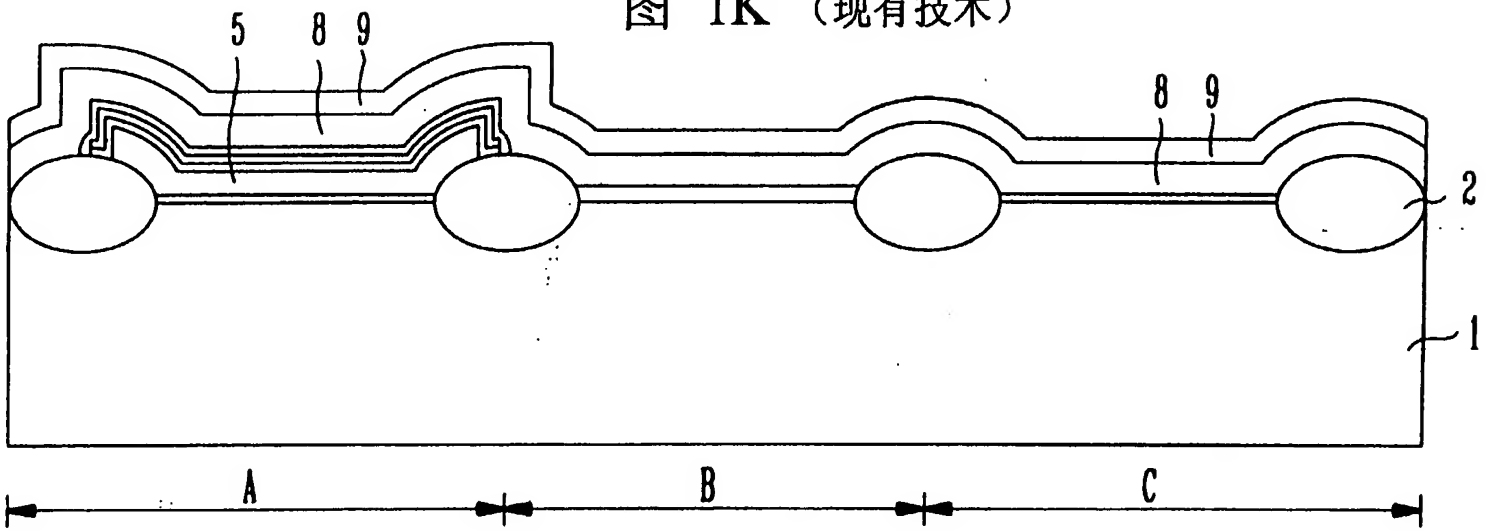


图 1L （现有技术）

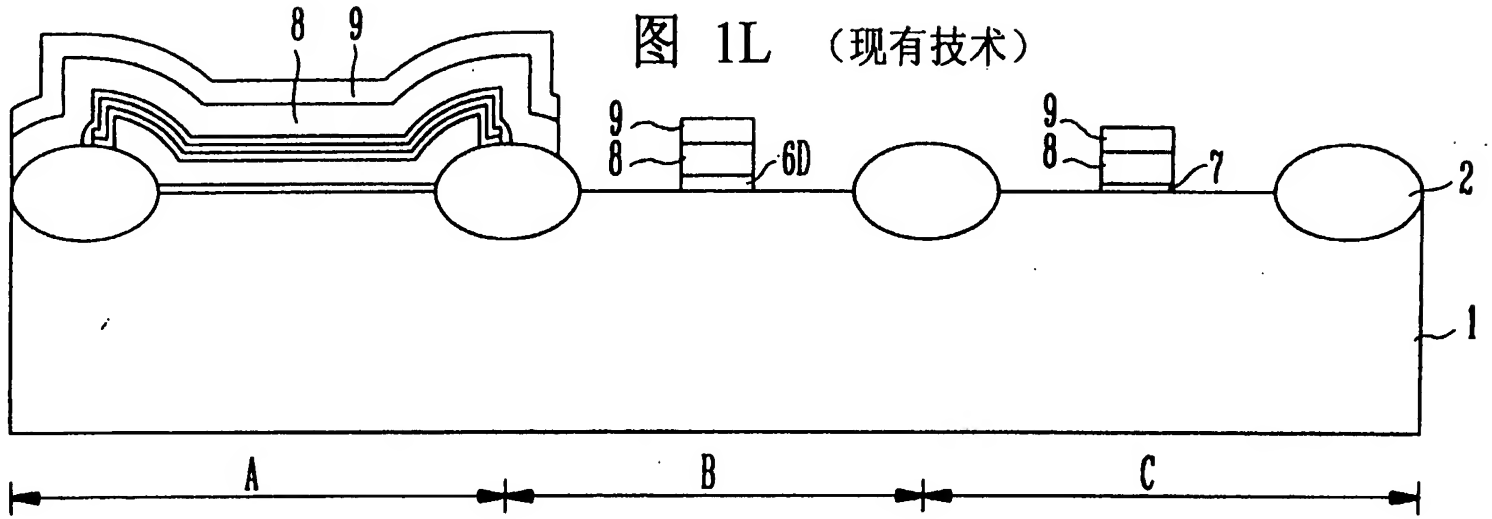


图 1M （现有技术）

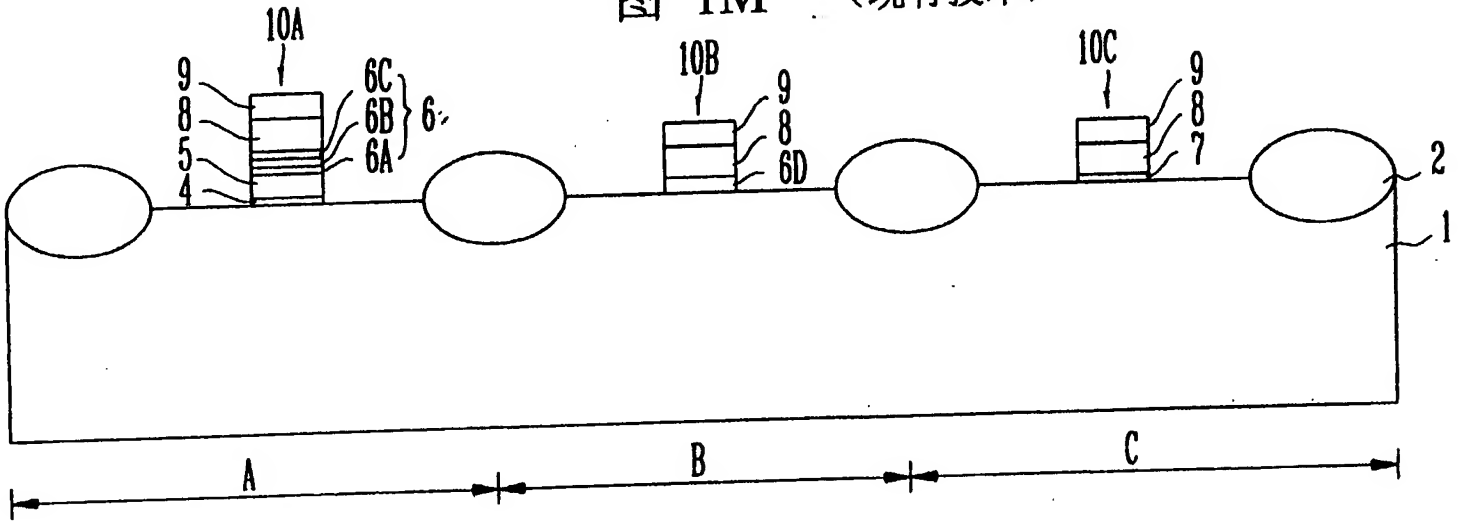


图 2A

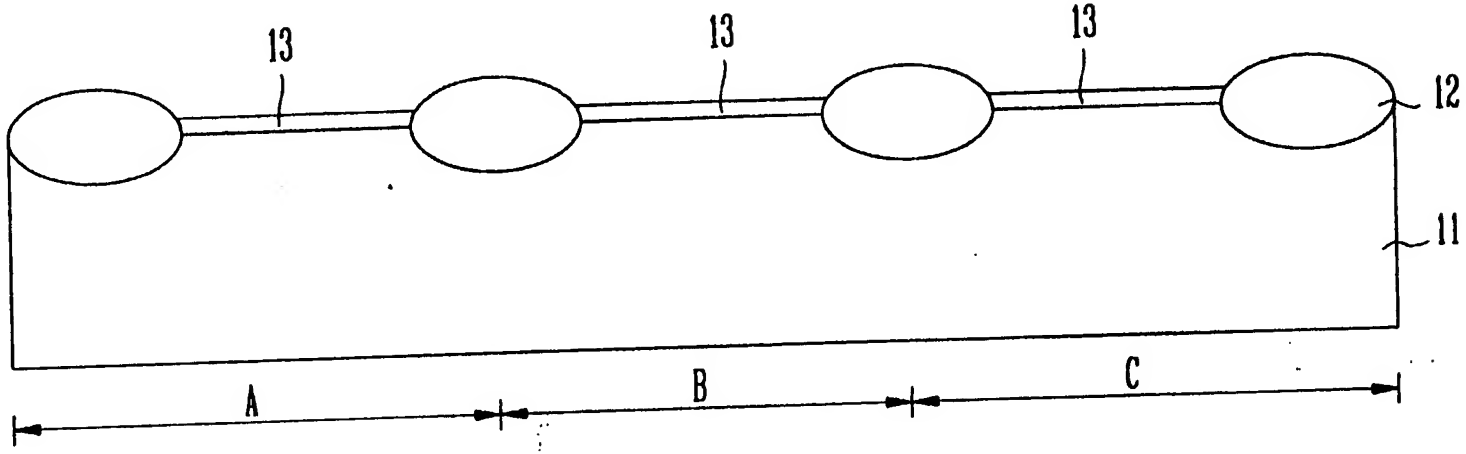


图 2B

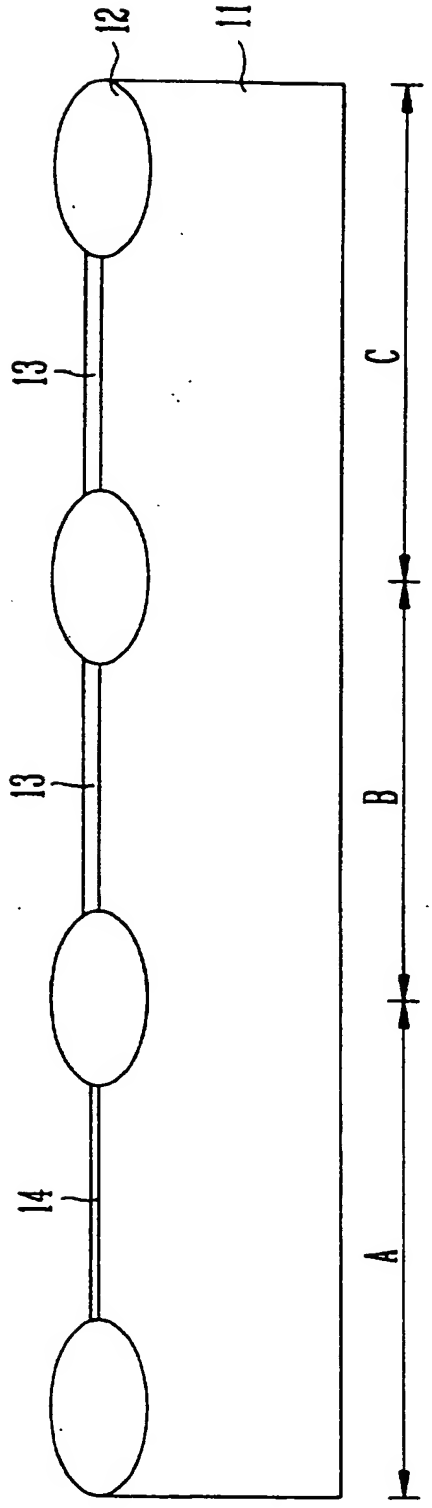


图 2C

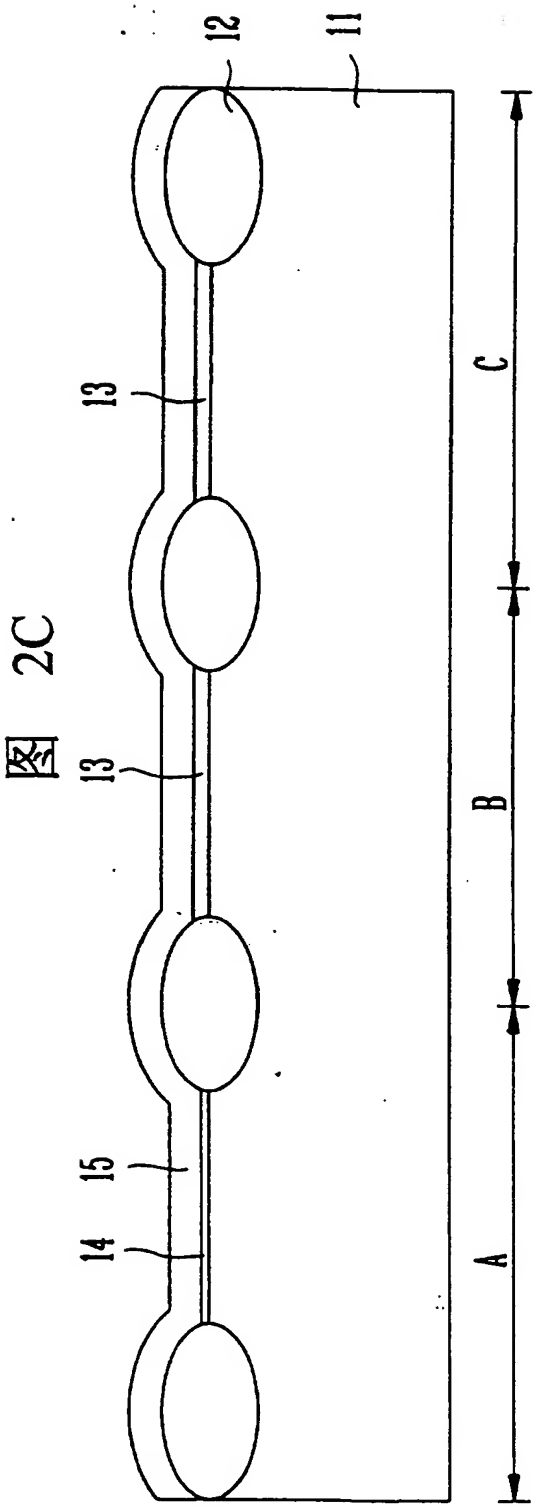


图 2D

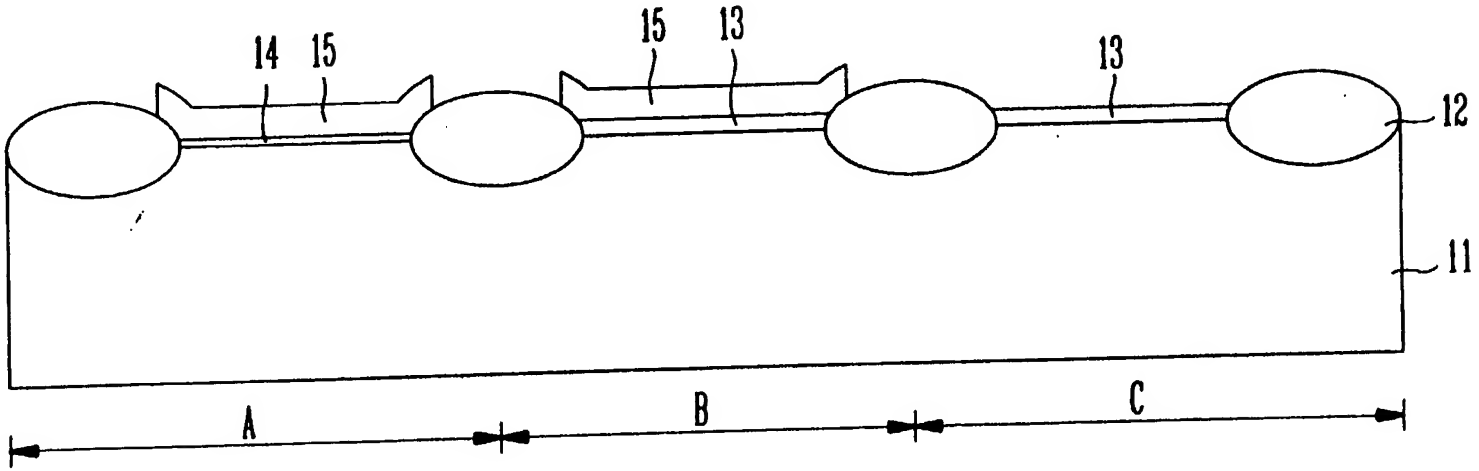


图 2E

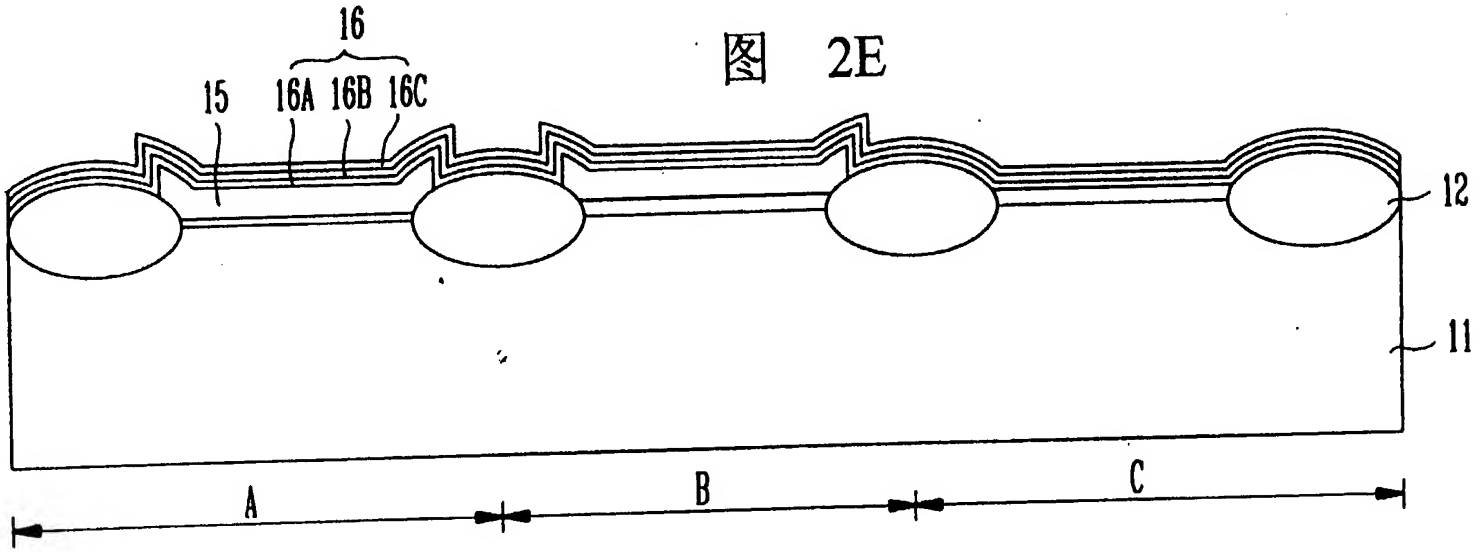


图 2F

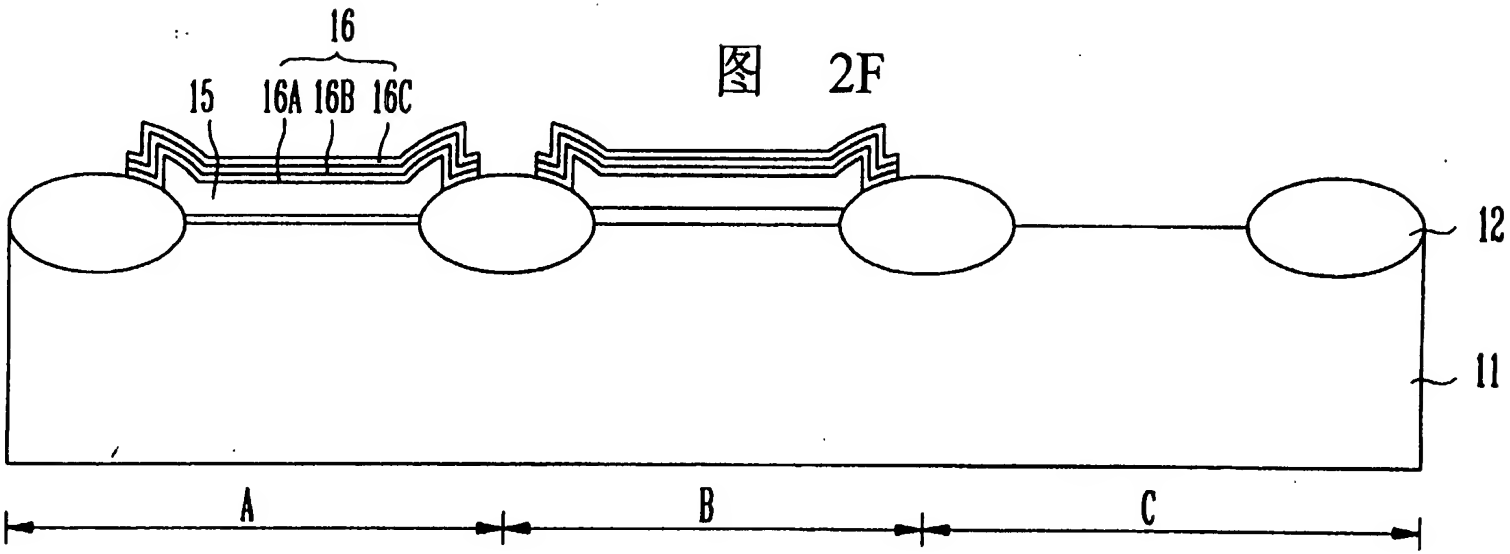


图 2G

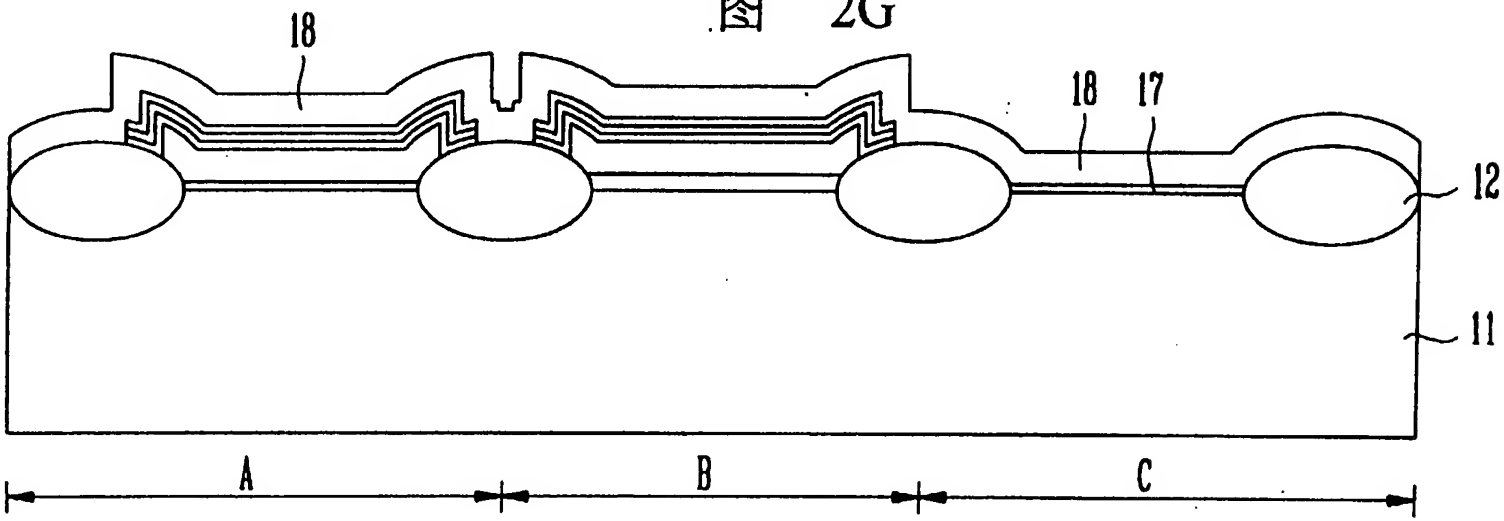


图 2H

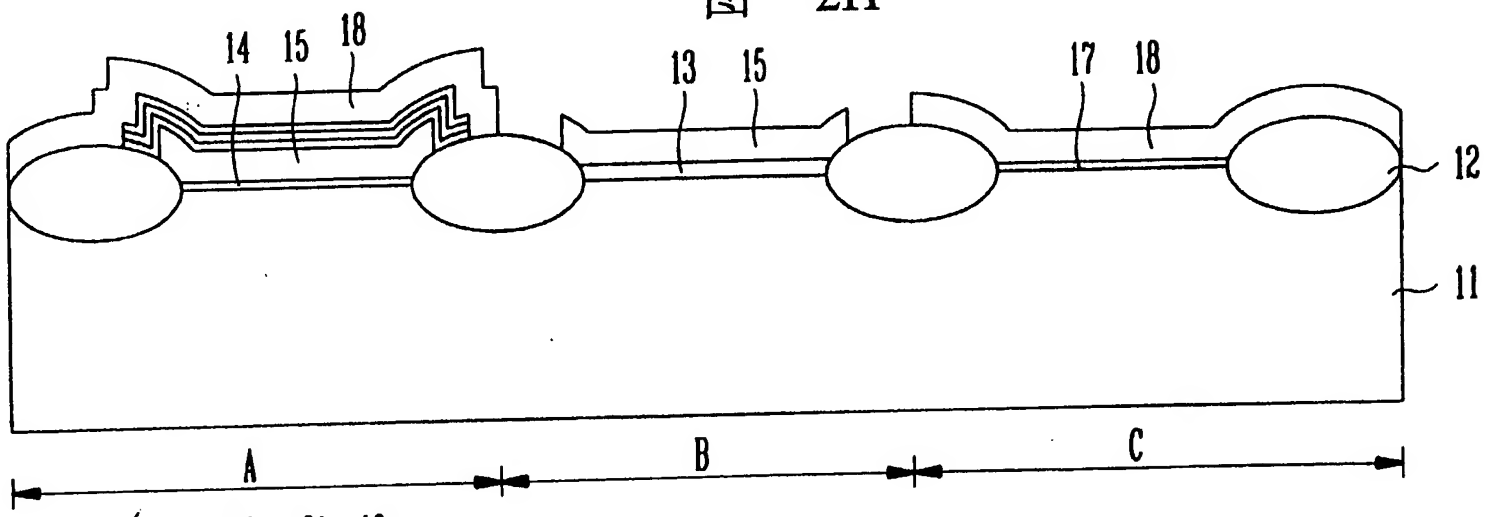
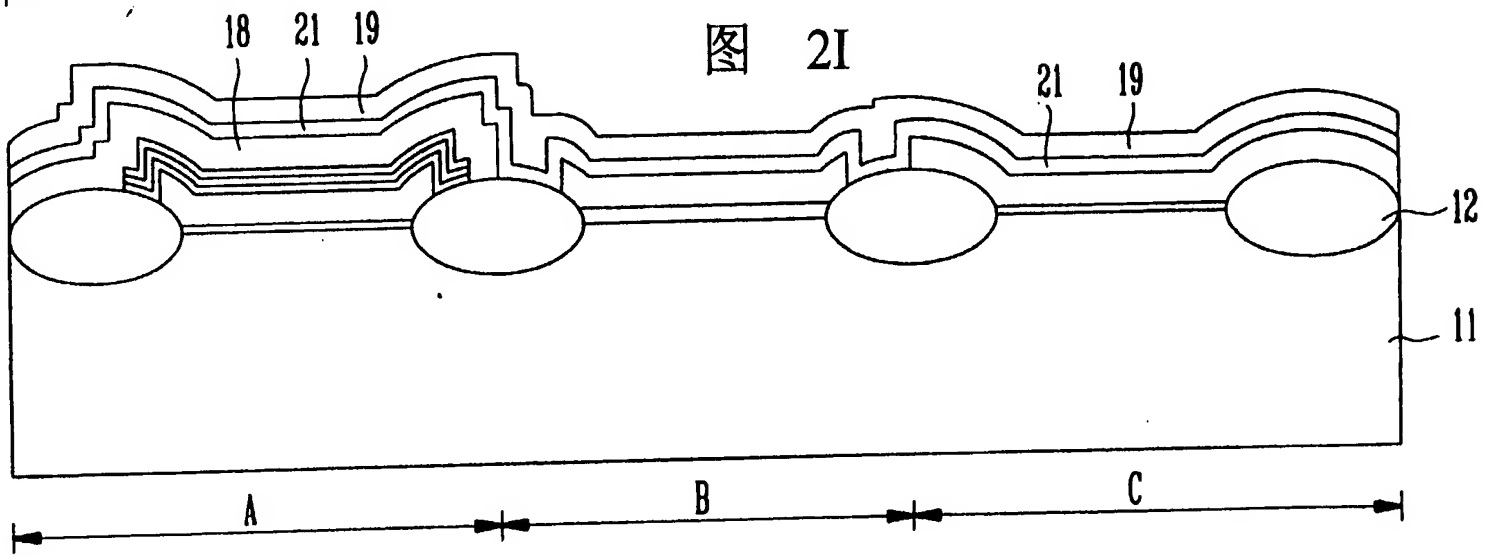


图 2I



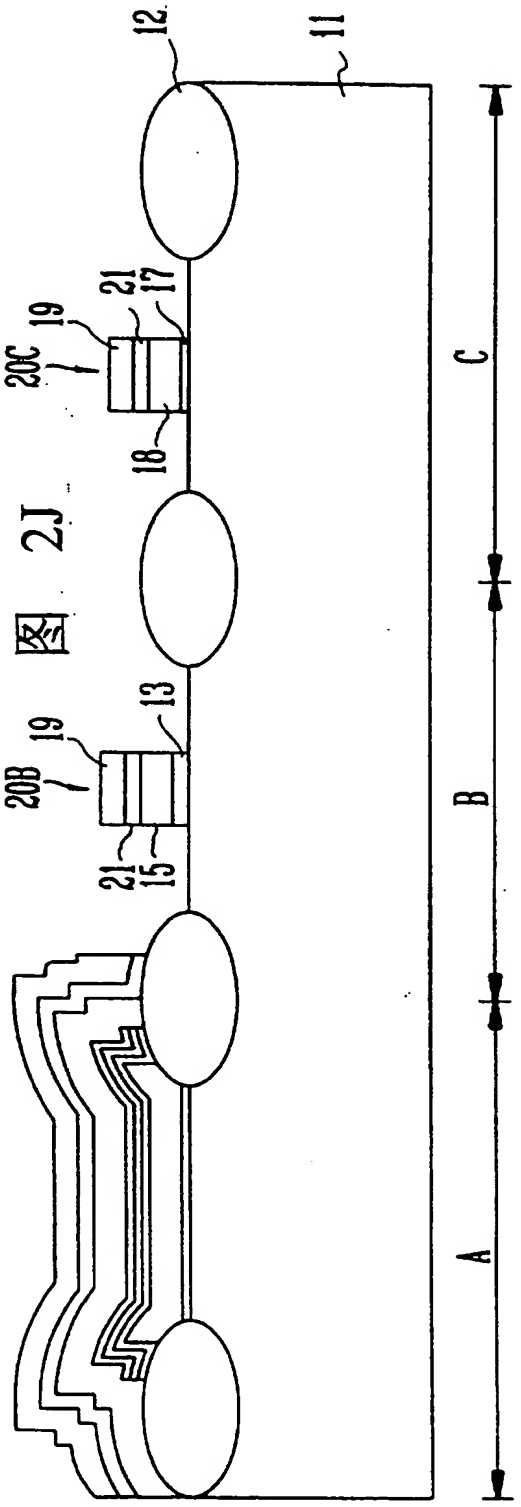

12
11
21
17
19
20C
18
C
13
19
20B
21
15
B
A

图 2J

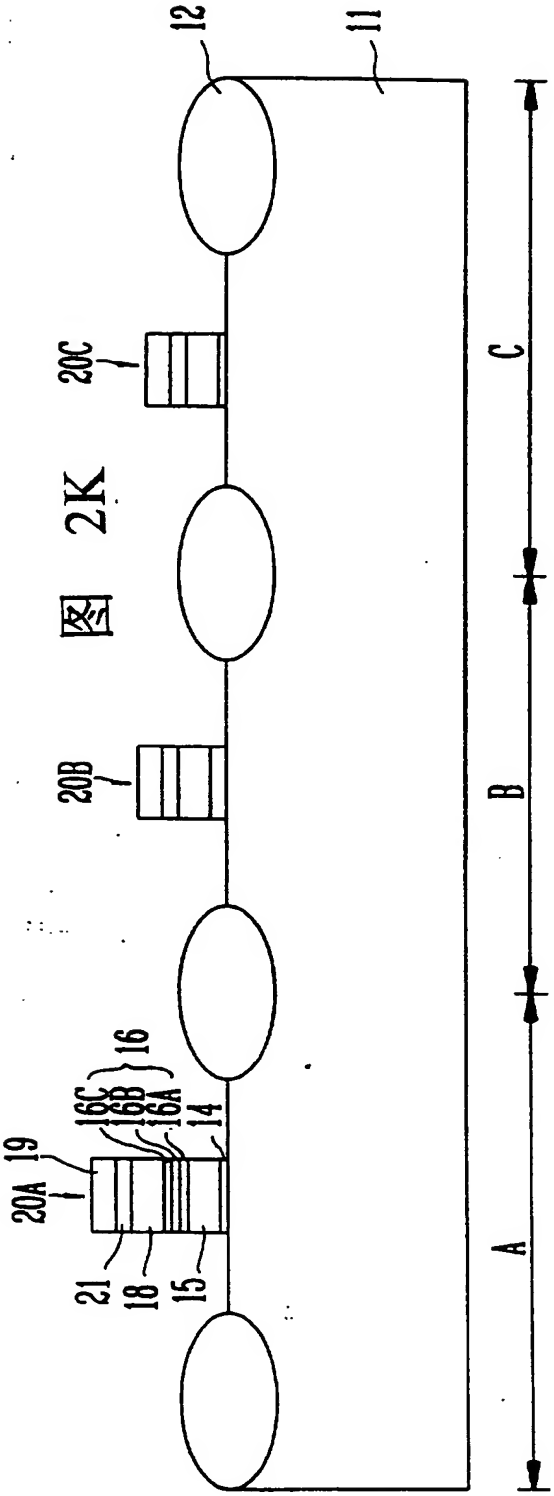

12
11
20C
C
20B
B
16
16C
16B
16A
14
19
20A
21
18
15
A

图 2K